



Issued by

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Acree Socware Center

IPR – Development

Designs listed below in silicon.

Circuit/block	Documentation available	Key data
LNA Low Noise Amplifier	Yes	6GHz BW, 13dB Gain, NF: 3,5-5
FFO Fixed Freq Oscillator	Yes	5,8GHz, -125dBc/Hz
PLL Phase Lock Loop	Yes	5-6GHz, 68dB spur suppression, Phase Noise: 129dBc/Hz
Phase Comparator Blocks	Yes	Phase/Frequency detector, charge pump and loop filter, sub-block of PLL was not tested separately.
VCO Voltage Controlled Oscillator	Yes	5,3-7,3GHz, Ph.Noise: -130dBc
VGA Variable Gain Amplifier	Yes	1.9-6GHz, Max -3dBm, 10step gain (3.5-26.5dB)
BBR-filters Baseband reconstruction filters	Yes	15MHz LP 4:th order elliptic Ripple: 0.5dB, Attenuation: 34dB IMRR<60dBc, 10mW, Robust
Analog RF Receive Front End 1 (FE1)	Yes	802.11 a/b/g Rx-chain including PLL
LNA	Yes	Parallel differential 50ohm, common gate architecture, 4-18dBgain (adjustable) NF: 5-6, 8GHz BW
Quadrature Down-Converter	Yes	Passive Multiband Quadrature mixer architecture, will not be tested separately
PLL Phase Lock Loop	Yes	Improved version of MPW1818, Integer-N, 2,4& 5Ghz, -127dBc/Hz, Non-programmable Can be tested separately
PA_1 Power Amp 1	Yes	Cascode bipolar Class A architecture, +18dBm/5GHz PA

PLL including full programmability and improved loop filter will be taped out in end of October -03. Design of a WCDMA version of the PLL in parallel.

Circuit/block	Documentation available	Key data/comments
Analog RF Front End 2 (FE2)	Ongoing	Complete 802.11a/b/g transceiver
Up-Converter & VGA	Ongoing	2-6GHz passive differential mixer structure, 0dBm VGA output
Rx Baseband	Ongoing	802.11 and WCDMA compatible
Tx Baseband Filter	Ongoing	802.11 a/b/g and WCDMA compatible 9MHz LP-filter, 40dB stop band att
PLL bias	Ongoing	SPI-IF and control registers
PLL	Ongoing	12 bit DA, DC offset cancellation loop

Designs listed below in silicon except for the ADC-M and -M2.

ADC-1 Analog to Digital Converter	Yes	Pipelined, 80 MS/s, 10 bit
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ADC-M	Ongoing	Supports 802.11a/b/g, pipelined, 40/20 MS/s, 10-bit, including digital correction
ADC-M2	No	Supports 802.11a/b/g and WCDMA, pipelined, 40/20 MS/s, 10-bit, including digital correction and multi-bit option
IFFT/FFT Inverse Fourier Transform/Fourier Transform	Yes	802.11 Tx
FEC Coder Forward Error Correction Coder	No	802.11 Tx
Scrambler	No	802.11 Tx
Interpolation filter	Yes	802.11 Tx
Interleaver	Yes	802.11 Tx

Designs listed below are ready for synthesizing.

Circuit/block	Documentation available	Key data/comments
Complete 802.11 OFDM Baseband-Tranceiver	Yes	The blocks below in this table are all included in this circuit.
Peak Clipper	Yes	802.11 Tx
Power control unit	Yes	802.11 Tx
Soft decision Viterbi decoder	Yes	802.11 Rx
Soft Demapper	Yes	802.11 Rx
Soft Deinterleaver	Yes	802.11 Rx
Packet detector, Frequency and Time sync.	Yes	802.11 Rx
Channel estimation phase tracking Equalization	Yes	802.11 Rx
Receiver channelization filter	Yes	802.11 Rx
Rx Quadrature error correction	Yes	802.11 Rx
Tx Quadrature error correction	Yes	802.11 Tx
AGC+RSSI	Yes	802.11 Rx
DC offset calculation and correction	Yes	802.11 Rx
Filter tuning controller	Yes	802.11 Tx/Rx
PA Bias control	Yes	802.11 Tx
Power detector calibration	Yes	802.11 Tx

About Acreo Socware Center

“ Acreo Socware Center, the hub of the Swedish Socware Cluster, with well experienced wireless IC and SoC designers and researchers focuses on wireless transceiver design from the system architecture level down to actual circuit level and has long experience and respected competence in radio specification and block level transceiver design. Along with a well equipped CAD and measurement lab, Acreo engineers design, model and characterize circuits and systems up to 50GHz fabricated in state-of-the-art processes. Acreo's design competence in RFIC, mixed signal, digital ASIC, and DSP allow for flexible fully implemented low power multi standard transceivers for the current and emerging wireless standards, e.g. 802.11a/b/g, 3G, UWB and more. “